UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/777,202	02/02/2001	Brian William Hughes	10004543-1	3035

7590 02/20/2004

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, CO 80527-2400

EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 02/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/777,202	HUGHES, BRIAN WILLIAM	
	Examiner	Art Unit	
	James C Kerveros	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Hedberg et al. (US 6026505), issued: February 15, 2000.

Regarding independent Claims 1, 9 and 16, Hedberg discloses a method and apparatus for an array built in self testing (ABIST) on a semiconductor chip (10) having an array of memory cells including column and row redundant lines, FIGS. 1 and 2, comprising:

Determining if the cells in each column groups (C0 to Cn) of the memory array (A) are defective, such as testing the array (A) along the columns (C0 to Cn) to identify a given number of faulty cells in each of the columns and storing the column addresses having the given number of faulty cells in address register (33) which receives the column and the row addresses of the cells of the array A.

Configuring the column groups of the stored column addresses including more than a predetermined number of defective cells in the address register (33), and also, shown in the circuit of FIG. 3, which identifies one of the array column lines (C0 to Cn) of FIG. 2 having a plurality of faulty or failed cells which is to be replaced by the redundant spare column line RC1.

Identifying by row remaining defective cells not replaced by the configuring column groups, as show in the circuit of FIG. 4, which can identify faulty or failed cells in two of the array row lines (R0 to Rm) of FIG. 2.

Configuring the rows of the memory array to be replaced by the two redundant row lines (RR1 and RR2) or can indicate that both of the redundant row lines RR1 and RR2 are to be used to replace two of the faulty array row lines R0 to Rm. The redundancy implementation processor 35 substitutes appropriate redundant column or row lines for faulty array column or row lines, (see column 2, lines 1-18).

Regarding Claims 2, 3, 10, 11, 17 and 18, Hedberg discloses testing memory cells as shown in flow chart (FIG. 6), including the steps of a screen test for finding hard faulty cell located along the column. A counting circuit FIG. 6, including (counter 38) counts the number of the defective cells identified in each of the column groups stored in the column fail address register circuit (22). If the column fail count, along any column, is greater than a threshold count (2), as set by the available number of row redundant lines, then the column count is set and the column address is stored or saved, (column 13, lines 30-54).

Regarding Claims 4, 12 and 19, Hedberg discloses generating at memory address using address counter 27, which generate the test data and address data, respectively, for the self-testing of the memory array (A) through the multiplexer 11. The test data is written into cells of the array A of the memory chip 10 and then read out to a data compression unit 31, where it is compared with a duplicate of the test data written into the cells of the array of the memory chip 10 from the data pattern generator 29. The results of the comparison are reduced to a single pass/fail or fault/no fault signal (column 3, line 4-13).

Regarding Claims 5-7,13-14 and 20, Hedberg discloses configuring the columns and rows of the memory array (A) FIGS. 1 and 2, using redundancy implementation processor 35 which substitutes appropriate redundant column or row lines for faulty array column or row lines. The address information stored in the two dimension failed address register (FIGS. 1, 3 and 4) is serially read out to the SCAN OUT terminal and then applied to the redundancy implementation processor 35 for substituting redundant column and row lines for the identified failed array column and row lines. Testing the memory array after performing the configuring column groups, using array built in self testing (ABIST) formed on the semiconductor chip (10) having an array of memory cells (A).

Regarding Claims 8 and 15 Hedberg discloses configuring column groups and configuring rows, which are performed by built-in self repair (BISR), such as processor 35, which includes a laser-fuse blowing device or an electrical latch setting circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James C Kerveros whose telephone number is (703) 305-1081. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James C Kerveros
Examiner
Art Unit 2133

By: _____

U.S. PATENT OFFICE
Examiner's Fax: (703) 746-4461
Email: james.kerveros@uspto.gov

Date: 2/17/04
Non-Final Rejection

Gregory J. Lamarre
for

Albert DeCady
Primary Examiner